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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/971,054	10/05/2001	Toshimitsu Tamagawa	103213-00041	1215

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EXAMINER	
JERABEK, KELLY L	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/971,054	TAMAGAWA, TOSHIMITSU	
	Examiner	Art Unit	
	Kelly L. Jerabek	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) *4 and 5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 4-5 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 4/7/2005.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 rejected under 35 U.S.C. 103(a) as being unpatentable over Hosier US 6,157,019 in view of Perry et al. US 6,548,323.

Re claim 1, Hosier discloses in figures 7-8 an interior and edge pixel layout of an image reading device consisting of a plurality of chips (10) mounted on a substrate (20). The device includes a plurality of photoelectric conversion elements (12) formed in rows on an IC chip (10) and a conductor layer (50) having openings for limiting light striking the photoelectric conversion elements (12) (col. 6, lines 12-65). Hosier also discloses an opaque layer (100) that is formed in an area extending from a photoelectric conversion element (12) located at each end of the IC chip (10) to a chip edge (col. 6, lines 24-65). However, although the Hosier reference discloses an opaque layer (100) it fails to distinctly state that the opaque layer is a metal conductor layer having substantially a same width as the conductor layer (50).

Perry discloses in figure 2 a light sensitive IC including an opaque material deposited on the semiconductor substrate lateral edges. Perry states that the opaque material can be a variety of metals (such as aluminum, titanium, etc.) and that the thickness of the opaque material layer will depend on the wavelength of light to be blocked (col. 5, lines 1-36). Therefore, it would have been obvious for one skilled in the art to have been motivated to include a metal opaque layer as disclosed by Perry with the same width as conductor layer (50) disclosed by Hosier as the opaque layer (100) disclosed by Hosier. Doing so would provide a means for blocking light (of the same wavelength as is blocked by conductor layer (50) at the edges of an IC (Perry: col. 5, lines 28-35).

Re claim 2, see claim 1.

Re claim 3, Hosier shows that the first conductor layer (50) and the opaque layer (100) are connected together by being formed continuously starting from the chip edge (figs. 7-8; col. 6, lines 12-65).

Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Hosier US 6,157,019 in view of Lee et al. US 5,34,216.

Re claim 6, Hosier discloses in figures 7-8 an interior and edge pixel layout of an image reading device consisting of a plurality of chips (10) mounted on a substrate (20). The device includes a semiconductor substrate (20) on which elements are formed, a plurality of photoelectric conversion elements (12) formed in rows on an IC chip (10) and a conductor layer (50) having openings for limiting light striking the photoelectric conversion elements (12) (fig. 2; col. 3, lines 52-67; col. 6, lines 12-65). However, although the Hosier reference discloses a semiconductor substrate it does not go into the details of the semiconductor construction. Specifically, Hosier fails to disclose an insulating layer formed over an entire surface of the IC chip and around the photoelectric conversion elements and a plurality of contact holes formed at predetermined intervals in the insulating layer so as to surround the openings, the contact holes serving to connect the metal conductor layer to the semiconductor substrate and preventing light from striking the photoelectric conversion elements

through openings other than the openings formed right above the respective photoelectric conversion elements.

Lee discloses in figure 3 an image sensor including a semiconductor substrate (30). The image sensor includes an insulating layer (37) formed over an entire surface of the sensor and a plurality of contact holes (37a,37b) formed at predetermined intervals in at least one row in the insulating layer (37) and surrounding openings in an optical shield conductor layer (42) (fig. 3; col. 4, lines 62 - col. 5, line 26). The contact holes (37a,37b) connect the metal conductor layer (42) to the semiconductor substrate (30) an simultaneously prevent light from striking the photoelectric conversion elements through openings other than the openings formed above the photoelectric conversion elements (col. 4, line 62 – col. 5, line 26). Therefore, it would have been obvious for one skilled in the art to have been motivated to include an insulation film formed on the surface of a substrate and contact holes as disclosed by Lee in the image reading device disclosed by Hosier. Doing so would provide a means for preventing blooming (Lee: col. 4, lines 62-66).

Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Hosier in view of Perry et al. and further in view of Lee et al.

Re claim 7, the combination of the Hosier and Perry references discloses all of the limitations of claim 2 above. However, although the Hosier reference discloses a semiconductor substrate it does not go into the details of the semiconductor

construction. Specifically, Hosier in view of Perry fails to disclose an insulating layer formed over an entire surface of the IC chip and around the photoelectric conversion elements and a plurality of contact holes formed at predetermined intervals in the insulating layer so as to surround the openings, the contact holes serving to connect the metal conductor layer to the semiconductor substrate and preventing light from striking the photoelectric conversion elements through openings other than the openings formed right above the respective photoelectric conversion elements.

Lee discloses in figure 3 an image sensor including a semiconductor substrate (30). The image sensor includes an insulating layer (37) formed over an entire surface of the sensor and a plurality of contact holes (37a,37b) formed at predetermined intervals in at least one row in the insulating layer (37) and surrounding openings in an optical shield conductor layer (42) (fig. 3; col. 4, lines 62 - col. 5, line 26). The contact holes (37a,37b) connect the metal conductor layer (42) to the semiconductor substrate (30) an simultaneously prevent light from striking the photoelectric conversion elements through openings other than the openings formed above the photoelectric conversion elements (col. 4, line 62 – col. 5, line 26). Therefore, it would have been obvious for one skilled in the art to have been motivated to include an insulation film formed on the surface of a substrate and contact holes as disclosed by Lee in the image reading device disclosed by Hosier in view of Perry. Doing so would provide a means for preventing blooming (Lee: col. 4, lines 62-66).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ishida et al. (US 6,590,611) discloses solid-state image-pickup devices and methods for motion detection. The information regarding a light shielding conductor layer is relevant material.

Hokari (US 5,514,887) discloses a silid state image sensor having a high photoelectric conversion efficiency. The information regarding a light shielding film is relevant material.

Hosier et al. (US 6,066,883) discloses a guarding for a CMOS photosensor chip. The information regarding a light shield is relevant material.

Hosier et al. (US 5,696,626) discloses a photosensitive silicon chip having a ridge rear an end photosite. The information regarding a light shield is relevant material.

Contacts

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kelly L. Jerabek whose telephone number is **(571) 272-7312**. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on **(571) 272-7308**. The fax phone number for submitting all Official communications is 703-872-9306. The fax phone number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at **(571) 273-7312**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLJ

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